

Notice of Allowability	Application No.	Applicant(s)	
	09/545,182	LIAO ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on 09/07/04.
2. ☒ The allowed claim(s) is/are 20-22,24-28 (claims 1-19, 23 have been canceled).
3. ☒ The drawings filed on 07 April 2000 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

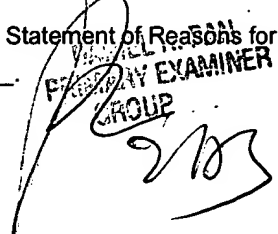
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____ |
|---|--|



 EXAMINER

Reasons for Allowance

Based on the prior art of record and the terminal disclaimer, the following are the reasons for allowance.

None of the prior art or record teaches:

- a) the combined features of the 0-5 bits encoding of the primary op code of 4, the 6-10 bits designating the floating point register for storing the 32 bit pair single precision value resulting from the paired of single floating point add instruction, the bits 11-15 designation of source register storing the pair floating values, the 16-20 bits floating point source register for the storage of the pair of 32 bit single precision values, the 21-25 bits encoding of reserved field of "0's", and a secondary op code 21, and the bit 31 for updating the condition register (claim 20 for the processor, claim 25 for the storage medium);
- b) the combined features of the pair of single scalar vector multiply add high instruction wherein the high order was used as scalar, the 0-5 bit encoding of primary op code of 4, the bits 6-10 designation of destination register for the result, the 11-15 designation of first floating point as the source for the first pair single precision, the 16-20 designation of the second floating point, the 21-25 as the third source pair of the 32 bit single precision, the 26-30 bits of the encoded secondary op code of 14 and bit 31 for the updating of the condition register (claim 21 for the processor, claim 26 for the storage medium);

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c) the combined features of the combined features of the pair of single scalar vector multiply add low instruction wherein the low order was used as scalar, the 0-5 bit encoding of primary op code of 4, the bits 6-10 designation of destination register for the result, the 11-15 designation of first floating point as the source for the first pair single precision, the 16-20 designation of the second floating point, the 21-25 as the third source pair of the 32 bit single precision, the 26-30 bits of the encoded secondary op code of 14 and bit 31 for the updating of the condition register (claim 22 for the processor, claim 27 for the storage medium);

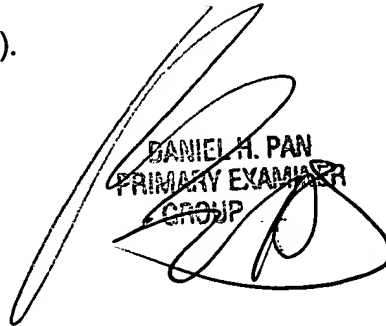
d) the decoding of the 32 bit paired of single floating point add instruction, the 0-5 bits of the encoding of the primary op code of 4, the 6-10 bits designation of floating point destination register for the 32 bit single precision resulting from the paired of add instruction, the 11-15 bits designation of floating point source register storing the 32 bit single precision floating point, the 16-20 bits designation of the source register, the 21-25 bits encoding of reserved field, the 26-30 encoding secondary op code of 21 and bit 31 of the updating of condition register, the specific bit designations for the floating point values for the 32 bit paired of single precision scalar vector multiply add high and low instructions (claim 24 for the decoder, claim 28 for the storage medium).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan


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